REMARKS

Present Status of the Application

The Office Action dated January 29, 2003 rejected all the pending claims 26, 28-32, 34-39 and 41 under 35 USC 103(a) as being unpatentable over the prior art relied upon the references of Oku et al. (US Patent No. 5,394,013), Chittipeddi et al. (US Patent No. 6,087,732), and Yuan (US Patent No. 5,838,043).

The remarks set forth in the Office Action have been carefully considered. However, for at least the reasons discussed hereafter, the Applicant disagrees with the Office Action rejections and believes that the claimed invention distinguishes over the prior art. Claims 26, 28, 30, 36, and 39 have been amended to more clearly distinguish over the cited references, without introduction of new matters.

In view of the following discussion, the Applicant earnestly solicits reconsideration and allowance of all the pending claims.

Discussion of the Office Action Rejections

Claim rejection under 35 USC 103

The Office Action rejected claims 26, 28, and 29 under 35 USC 103(a) as being unpatentable over Oku et al. in view of Chittipeddi et al.

The Office Action rejected claims 30-32,34-39 and 41 under 35 USC 103(a) as being unpatentable over Oku et al. in view of Chittipeddi et al. and further in view of Yuan.

These rejections are respectfully traversed.

As described in claims 26 and 28, a specific feature of the invention is the provision of

metal layers that are concentric to reduce the capacitance by reducing the area of the substrate overlapped by the metal layers.

As discussed in the previous responses, neither Oku et al. nor Yuan relied upon in the Office Action disclose or suggest the arrangement of *concentric* metal layers in a bond pad structure. Nor the newly cited reference of Chittipeddi et al. properly describes a bond pad structure including concentric metal layers. As described in FIG. 3 and 4 and related text col.4:14-66 and col. 5:12-60, Chittipeddi et al. teaches a bond pad structure that comprises *radial* metal layers 301-304 and 401-404 shaped rectangular and triangular. Clearly, the *radial arrangement* of these metal layers 301-304 and 401-404 differs from the metal layers of the invention that, as recited in the claims, are *concentric* relative to one another.

For at least the above reasons, it is submitted that even if the cited references are combined with one another, they still would have failed to adequately meet the claimed invention in which *concentric* metal layers are provided. Accordingly, claims 26, 28, and 29 patently distinguish over the prior art references, and withdrawal of the improper rejection is respectfully requested.

The above same reasons apply to claims 30-32, 34-39, and 41 that, therefore, also patently distinguish over the cited references.

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 26, 28-32, 34-39 and 41 of the invention patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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VERSION WITH MARKED-UP AMENDMENTS TO SHOW THE AMENDMENTS MADE

In The Claims

The claims have been amended as follows.

26 (Amended) A low-capacitance bonding pad for a semiconductor device, comprising:

a substrate;

a stack of metal layers alternating with dielectric layers on the substrate, wherein the metal layers are coupled with one another by a plurality of via plugs in the dielectric layers, the via plugs being placed in alternating manner with respect to one another through the stack, and the metal layers are ~~in a~~ concentric ~~circle arrangement~~ to reduce the capacitance by reducing the area of the substrate overlapped by the metal layers;

an uppermost metal layer positioned on the stack and electrically connected to the stack, wherein an area of each metal layer in the stack is smaller than that of the uppermost metal layer; and

a passivation layer having a bonding pad opening positioned on the uppermost metal layer for externally electric connection.

28. (Amended) A low-capacitance bonding pad for a semiconductor device, comprising:

a substrate;

a stack of metal layers alternating with dielectric layers on the substrate, wherein the metal layers are coupled with one another by a plurality of via plugs through the dielectric layers and are ~~placed in a~~ concentric ~~circle arrangement,~~ to reduce the capacitance by reducing the area of

the substrate overlapped by the metal layers;

an uppermost metal layer positioned on the stack and electrically connected to the stack; and

a passivation layer having a bonding pad opening on the uppermost metal layer for externally electric connection.

30. (Amended) A low-capacitance bonding pad for a semiconductor device, comprising:

a substrate having a well;

a doped region formed in the well as a diffusion region; and

a bonding pad on the substrate, the bonding pad comprising a stack of metal layers alternated with dielectric layers and an uppermost metal layer, the metal layers and the uppermost metal layer being electrically connected to one another by a plurality of via plugs through the dielectric layers, wherein the bonding pad is aligned with the doped region and the metal layers are ~~in a~~ concentric ~~circle arrangement~~ to reduce the capacitance by reducing the area of the substrate overlapped by the metal layers.

36. (Amended) A semiconductor device, comprising:

a substrate having a well;

a doped region formed in the well as a diffusion region;

a bonding pad on the substrate, the bonding pad ~~being~~ comprising a stack of metal layers alternated with dielectric layers and an uppermost metal layer, the metal layers and the uppermost metal layer being electrically connected to one another by a plurality of via plugs through the dielectric layers, wherein the bonding pad is aligned with the doped region, and wherein the metal layers in the stack are ~~in a~~ concentric ~~circle arrangement~~ to reduce the area of

the substrate overlapped by the metal layers; and

a semiconductor device under the bonding pad.

39. (Amended) A semiconductor device, comprising:

a substrate having a well;

a doped region formed in the well as a diffusion region;

a bonding pad on the substrate, the bonding pad comprising a stack of metal layers alternated with dielectric layers and an uppermost metal layer, the metal layers and the uppermost metal layer being electrically connected to one another by means of a plurality of via plugs, wherein the bonding pad is aligned with the doped region; and wherein an area of each metal layer in the stack is smaller than that of the uppermost metal layer, and the metal layers are ~~in a~~ concentric ~~circle arrangement~~ to reduce the area of the substrate overlapped by the metal layers; and

a semiconductor device under the bonding pad.